connecting semiconductor devices in said semiconductor wafer to ball grid arrays on said dielectric layer; and

subsequently, dicing said layered assembly.

Cancel claims 24-34, without prejudice.

REMARKS

Claim 11 has been amended. Non-elected claims 24-34 have been canceled. Claims 1-23 and 35-38 remain in the application. Applicants reserve the right to pursue the original claims and other claims in this application and in other applications.

Claims 1, 5, 6, 8 and 9 are rejected under 35 U.S.C. § 102 as being anticipated by Mizuno. Applicants respectfully traverse the rejection and request reconsideration. Claim 1 recites a "method of making semiconductor device packages." The method includes the steps of "testing semiconductor devices in [a] wafer" and, "subsequently, dicing [a] layered assembly." Mizuno fails to disclose or suggest the step of "testing semiconductor devices in said wafer." Applicants do not understand the Office Action's reference to column 5, lines 1-12 of the Mizuno patent, which has nothing to do with "testing semiconductor devices." The step of "testing semiconductor devices in said wafer," before the dicing of the layered assembly, is an important aspect of the claimed invention. Please refer to Applicants' specification, page 2, lines 18+. Claims 2-10 depend from independent claim 1 and are believed to be allowable along with claim 1 and for other reasons.

Claims 11-18 are rejected under 35 U.S.C. § 102 as being anticipated by Heo. Applicants respectfully traverse the rejection and request reconsideration. As noted in the Office Action, Heo refers to certain conductive elements, but Heo nowhere discloses or suggests the "stiff metal layer" of amended claim 11. The "stiff metal layer" is an important aspect of the claimed invention. Please refer, for example, to the discussion of

the Heo patent on page 2 of Applicants' specification. Claims 12-18 depend from independent claim 11 and are believed to be allowable along with claim 11 and for other reasons.

Claims 36-38 are rejected under 35 U.S.C. § 103 as being unpatentable over Mizuno in view of Kobayashi. Applicants respectfully traverse the rejection and request reconsideration. Independent claim 35 recites "[a] method of handling a plurality of semiconductor devices arrayed in a . . . wafer." The method includes the step of "testing said semiconductor devices through . . . ball grid arrays." As discussed above, Mizuno fails to disclose or suggest the concept of testing semiconductor devices while they are still arrayed in the wafer. Kobayashi is cited in the Office Action for other features. Accordingly, claim 35 should be allowable over Mizuno in view of Kobayashi. Claims 36-38 depend from independent claim 35 and are believed to be allowable along with claim 35 and for other reasons.

The allowance of claims 19-23 is gratefully acknowledged. In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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MARK UP VERSION SHOWING CHANGES MADE

11. (Amended) A method of making semiconductor device packages, comprising:

forming a layered assembly by attaching a semiconductor wafer and a stiff metal layer to a dielectric layer;

connecting semiconductor devices in said semiconductor wafer to ball grid arrays on said dielectric layer; and

subsequently, dicing said layered assembly.